Gate Bias Stress in Pentacene Field-Effect-Transistors: Charge Trapping in the Dielectric or Semiconductor

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Gate bias stress instability in organic field-effect transistors (OFETs) is a major conceptual and device issue. This effect manifests itself by an undesirable shift of the transfer characteristics and is associated with long term charge trapping. We study the role of the dielectric and the semiconductor separately by producing OFETs with the same semiconductor (pentacene) combined with different dielectrics (SiO$_2$ and Cytop). We show, it is possible to fabricate devices which are immune to gate bias stress. For other material combinations, charge trapping occurs in the semiconductor alone, or in the dielectric.

Keywords: Gate Bias Stress, trapping, pentacene, Cytop, current instability, degradation, interface, threshold voltage shift

Charge trapping in organic field-effect transistors (OFETs) happens on various time scales. Trapping due to gate bias stress is a relatively slow process which takes place on the timescale of fractions of seconds up to several days, posing a challenge to the experiment as well as the conceptual understanding. Previous studies produced OFETs with a gate bias stress stability comparable to that of a-Si thin-film-transistors (TFT)[1].

Several mechanisms have been proposed to explain the threshold-voltage shift under gate bias stress: (i) trapping of charges in the bulk of the semiconductor[2], (ii) trapping in disordered areas of the semiconductor[3], (iii) trapping in regions in-between crystalline grains of the semiconductor[4], (iv) trapping in states at the semiconductor/dielectric interface[5] and (v) formation of bipolarons in the semiconductor[6,7] as summarized by Sharma et al.[8]. From temperature dependent measurements gate bias stress effects were found to be thermally activated with a comparable activation energy of $E_\tau \approx 0.6$ eV over a wide range of organic materials[9]. This has been taken as an indication that the underlying process is the same for all tested organic materials. Recently, charges have been shown to be trapped in the SiO$_2$ as the gate dielectric[10]. Although the mechanism behind this trapping is still unclear, Sharma et al.[8,11] explain it by a proton migration mechanism involving water, whereas Lee et al.[12] assume direct drift/diffusion of holes into the dielectric.

Here we present a comparative study of OFETs with either SiO$_2$ or Cytop (a highly hydrophobic fluoropolymer) as dielectric and with pentacene thin-films or single crystals as semiconductor. The focus is on a quantitative measurement of the threshold voltage shift ΔV_{th} over an extended time range (10^{-1} to 10^3 s) in response to an applied gate voltage. By combining the semiconductor either in thin-film or single crystal form with the two different gate dielectrics, charge trapping can either be completely suppressed in the OFET, or it occurs (a) in
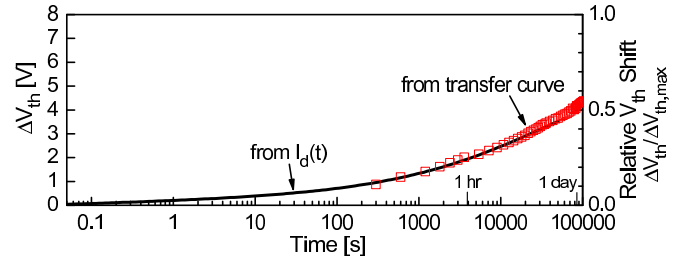

FIG. 1. The influence of the Gate Bias Stress on the threshold Voltage V$_{th}$ has been measured in two ways: (i) the decrease of I$_d$(t) over time has been measured, (ii) V$_{th}$ has been calculated from the shift of the transfer curve over time. These two methods agree with each other in determining the threshold voltage shift ΔV_{th}.

the semiconductor or (b) in both the semiconductor and the dielectric.

Usually the threshold voltage shift ΔV_{th}(t) is analyzed by measuring transfer curves at various times. With a gate bias applied in between. This straightforward measurement has some drawbacks, however: Firstly, it is slow, therefore information about the first few, or even fraction of seconds is not accessible. Secondly, some devices, especially thin-film-transistors (TFTs) do not show a linear regime and thus deriving a threshold voltage is not straightforward, even as the transfer curve clearly shifts.

Therefore we use a different method to measure the gate bias stress influence over time. Instead of measuring a full transfer curve, the evolution of the drain current I$_d$ is measured at a certain applied gate voltage V$_g$ and source-drain voltage V$_d$[13]. The decrease of I$_d$(t) over time can be translated into a shift of the transfer curve (and therefore V$_{th}$). These two methods give the same result (Fig. 1). A "relative threshold voltage shift" $\frac{\Delta V_{th}}{\Delta V_{th,max}}$ is used to compare different devices. $\Delta V_{th,max}$ is given by the difference between the initial threshold voltage V_{th}(t=0) and the applied gate bias $V_{g,appl}$.

The 3 devices, differing in their semiconductor/dielectric
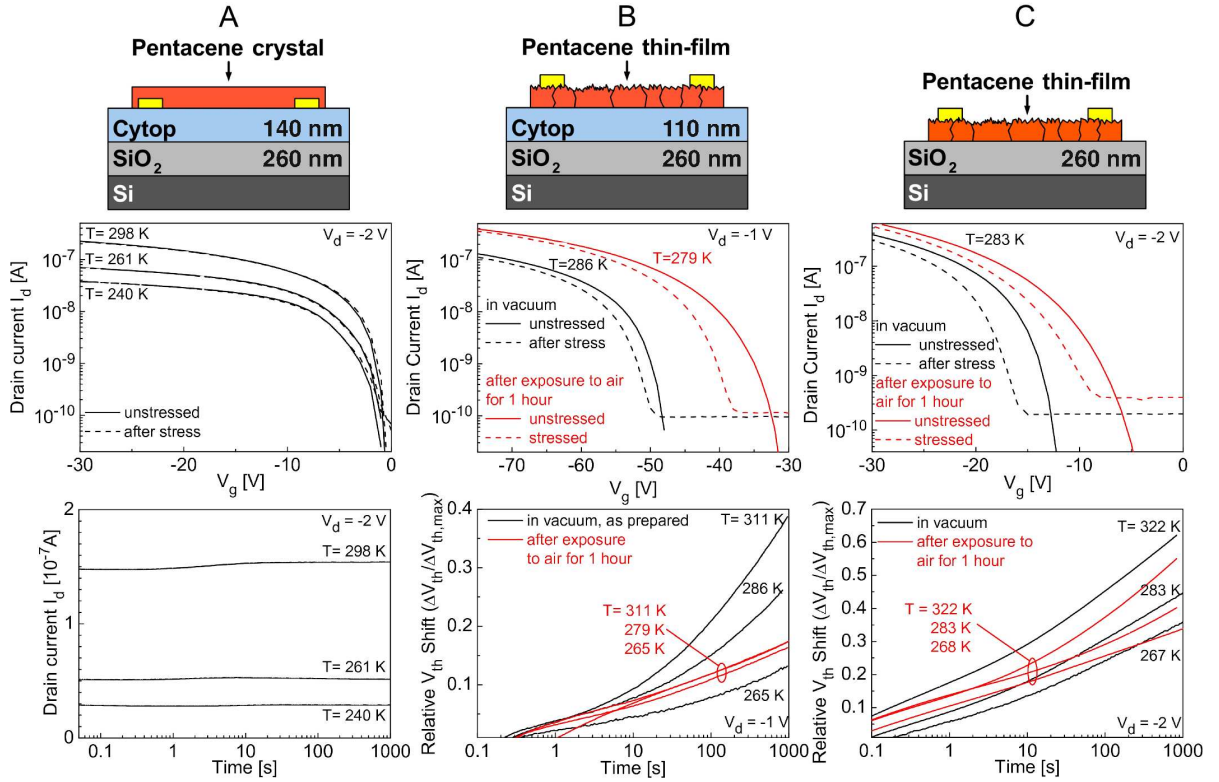
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FIG. 2. Different mechanism at work resulting in gate bias stress effects. This compilation of graphs show the device setup (first row), the measured transfer curves (middle row) and the drain current $I_d(t)$ or relative threshold voltage shift over time (bottom row).

Device A: (C_i=6.6×10^{-5} F/m^2) Transfer curves at various temperatures before and after stress do not show any gate bias stress effects. The same for the measurement of the drain current. $I_d(t)$ is stable over the measured time with a slight increase which is attributed to self heating of the device.

Device B: (C_i=7.4×10^{-5} F/m^2) Shows a gate bias stress effect in the transfer curves. The time and temperature dependent measurement of the relative threshold voltage shift (bottom row) shows this effect to strongly depend on temperature. After exposure to ambient air for 1 hour, the underlying process for long term charge trapping completely changes and becomes temperature independent.

Device C: (C_i=1.3×10^{-4} F/m^2) Also shows gate bias stress visible in the transfer curve and the time/temperature dependent measurement. After exposure to air, the the gate bias stress effect stays strongly temperature dependent.

combination, are shown in figure 2. Device A is a flip-crystal OFET[14,15] with Cytop as the gate dielectric[16,17] and the crystals grown according to Kloc et al.[18]. For Devices B and C, the pentacene thin-films and the gold contacts have been evaporated in 10^{-7} mbar vacuum, the devices are transferred to the attached probe station, where they can be exposed to various atmospheres in a controlled way: in this study 1 hour of air at 0.2 bar was chosen. The single crystal device has been exposed to ambient air during sample preparation.

The devices have been analyzed as follows: A transfer-curve has been measured using a series of short V_g pulses (50 ms) in order to minimize the stress. Afterwards the source-drain current, $I_d(t)$, has been measured at a fixed V_g and V_d. At the end, again a pulsed transfer-curve has been measured, with a V_g offset between two pulses equal to the previously applied gate bias during stress-

ing, to check that the shape of the transfer curve has been conserved. We repeat these series of measurements at several temperatures. In addition the transfer characteristics are the basis for calculating the trap density-of-states (trap DOS) in the band-gap using a FET simulator developed by Oberhoff et al.[19], applied to other OFET configurations previously[20–22].

For Device A, the single crystal OFET, most significantly no gate bias stress effect is visible after stressing for 17 minutes at V_g=-20 V. Even when monitoring the source-drain current during applied gate voltage (Fig. 2 bottom) no reduction of the current is seen which would indicate stress effects. The hole mobility is ≈ 0.6 - 0.7 cm^2/Vs at room temperature. Additionally the trap DOS is very low (Fig. 3). Therefore, the combination of Cytop together with a pentacene single-crystal results in an extremely good interface[16,23], and long term charge
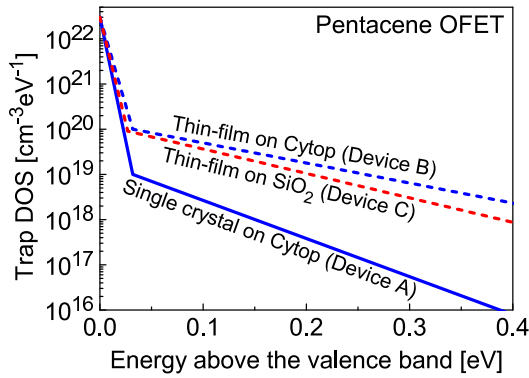
FIG. 3. Comparison of different trap density-of-states for the 3 devices as calculated from transfer curves taken at different temperatures. The two thin-film devices have essentially the same trap DOS, whereas in the single crystal OFET the trap DOS is one to two orders of magnitude lower.

trapping is effectively suppressed in the dielectric. Obviously, no long term charge trapping occurs in the pentacene crystal either.

Device B, consisting of polycrystalline thin-film evaporated onto Cytop dielectric, shows gate bias stress effect. The extensive study of $\Delta V_{th}(t)$ reveals long term charge trapping to be strongly temperature dependent when the device is always kept in vacuum. From Device A we learned that charges are not trapped in the Cytop, and thus in Device B it occurs in the polycrystalline pentacene thin-film. Exposing Device B to air causes several changes. The mobility approximately doubles from 0.08 to 0.15 cm^2/Vs. Turn-on and threshold voltage $V_{th}(0)$ are significantly reduced. A more peculiar effect after exposure to air is seen when analyzing the temperature dependence of $\Delta V_{th}(t)$: the gate bias stress effect becomes essentially independent of temperature.

Device C shows similar turn-on behavior as Device B except at a much lower initial threshold voltage. Again ΔV_{th} due to gate bias stress is clearly visible in the transfer curves as well as in the threshold voltage shift over time. In passing, we note $\Delta V_{th}(t)$ to be stronger by a factor of 2 in Device C compared to Device B. Exposure to air increases the mobility (0.1 to 0.15 cm^2/Vs) and shifts the transfer curves to lower gate voltage. After exposure to air, the relative threshold voltage shift remains temperature dependent, in contrast to Device B, where the temperature dependence vanishes after exposure to air.

For further discussion, we would like to point out that the mobilities in the two thin-film devices are essentially identical and the trap DOS is similar too (Fig. 3). Thus from the conduction measurements before and after exposure to air these two films behave the same. Therefore it appears that whatever their morphological differences may be, they have no effect on the DC properties. Additionally, as Miyadera et al.[24] have found, the morphology of a pentacene film does not significantly change the long term trapping dynamics, thus the distinctly different behavior between Device B and C can not be attributed to a different film morphology.

The shift of the initial threshold voltage after exposure to air in Devices B and C is due to filling of charge traps, where oxygen acts as a hole donor. This shift is the same for Device B and C, in terms of induced charge (5×10^{18} e/cm^3), assuming a channel thickness of 1.5 nm. This is in quantitative agreement with the analysis by Kalb et al.[25], where trap states were created in the band gap due to oxygen exposure. Therefore, since long term charge trapping in devices with SiO$_2$ is known to be due to trapping in the SiO$_2$[10], exposure to oxygen which alters the semiconductor only, does not change this mechanism significantly. But in devices where long term charge trapping occurs in the semiconductor, changes of the semiconductor due to oxygen exposure can be expected to alter this mechanism. This is exactly what has been observed as the difference between Device B and C.

In Summary we have shown that it is possible to fabricate OFETs using Cytop and pentacene single crystals which do not show gate bias stress effects and have a very low trap density. The device with pentacene thin-films on Cytop does show gate bias stress effects which is due to trapping of charges in the semiconductor. When this device is exposed to air, the gate bias stress effect becomes temperature independent which is an additional hint of the different origin of the charge trapping mechanism when compared to the OFET with SiO$_2$ as gate dielectric. Therefore we conclude that long term charge trapping occurs in the semiconductor thin-film if charge trapping in the dielectric is suppressed.

[1] T. Umeda, D. Kumaki, and S. Tokito, Organic Electronics **9**, 545 (2008).

[2] J. B. Chang and V. Subramanian, Applied Physics Letters **88**, 233513 (2006),.

[3] A. Salleo, F. Endicott, and R. A. Street Applied Physics Letters **86**, 263505 (2005).

[4] M. Tello, M. Chiesa, C. M. Duffy, and H. Sirringhaus, Advanced Functional Materials **18**, 3907 (2008).

[5] R. A. Street, M. L. Chabinyc, F. Endicott, and B. Ong, Journal Of Applied Physics **100**, 114518 (2006).

[6] R. A. Street, A. Salleo, and M. L. Chabinyc, Physical Review B **68**, 85316 (2003).

[7] G. Paasch, J. Electroanal. Chem. **600**, 131 (2007).

[8] A. Sharma, S. Mathijssen, E. Smits, M. Kemerink, D. de Leeuw, and P. Bobbert, Physical Review B **82**, 1 (2010) BibitemShutNoStop

[9] S. G. J. Mathijssen, M. Colle, H. L. Gomes, E. C. P. Smits, B. de Boer, I. McCulloch, P. A. Bobbert, and D. M. de Leeuw, Advanced Materials **19**, 2785 (2007).

[10] S. G. J. Mathijssen, M.-J. Spijkman, A.-M. Andringa, P. A. van Hal, I. McCulloch, M. Kemerink, R. A. J. Janssen, and D. M. de Leeuw, Advanced Materials **22**, 5105 (2010).

[11] A. Sharma, S. G. J. Mathijssen, T. Cramer, M. Kemerink, D. M. de Leeuw, and P. A. Bobbert, Applied Physics Letters **96**, 103306 (2010).

[12] B. Lee, a. Wan, D. Mastrogiovanni, J. Anthony, E. Garfunkel, and V. Podzorov, Physical Review B **82**, 3 (2010).

[13] C. C. Shih, Y. S. Lee, K. L. Fang, C. H. Chen, and F. Y. Gan, Ieee Transactions On Device And Materials Reliability **7**, 347 (2007).

[14] R. W. I. de Boer, M. E. Gershenson, a. F. Morpurgo, and V. Podzorov, Physica Status Solidi (a) **201**, 1302 (2004).

[15] J. Takeya, C. Goldmann, S. Haas, K. P. Pernstich, B. Ketterer, and B. Batlogg, Journal of Applied Physics **94**, 5800 (2003),.

[16] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, and B. Batlogg, Applied Physics Letters **90**, 92104 (2007).

[17] M. P. Walser, W. L. Kalb, T. Mathis, T. J. Brenner, and B. Batlogg, Applied Physics Letters **94**, 53303 (2009).

[18] C. Kloc, P. Simpkins, T. Siegrist, and R. Laudise, Journal of crystal growth **182**, 416 (1997),.

[19] D. Oberhoff, K. P. Pernstich, D. J. Gundlach, and B. Batlogg, Ieee Transactions On Electron Devices **54**, 17 (2007).

[20] W. L. Kalb and B. Batlogg, Phys. Rev. B **81**, 35327 (2010).

[21] W. L. Kalb, S. Haas, C. Krellner, T. Mathis, and B. Batlogg, Physical Review B **81**, 155315 (2010).

[22] K. P. Pernstich, D. Oberhoff, C. Goldmann, and B. Batlogg, Applied Physics Letters **89**, 213509 (2006).

[23] M. Uno, Y. Tominari, and J. Takeya, Organic Electronics **9**, 753 (2008).

[24] T. Miyadera, S.-D. Wang, T. Minari, K. Tsukagoshi, and Y. Aoyagi, Applied Physics Letters **93**, 33304 (2008).

[25] W. L. Kalb, K. Mattenberger, and B. Batlogg, Physical Review B **78**, 1 (2008).